In the Claims:

1. (Original) A composite spacer for use with a split gate flash memory cell on a substrate, comprising:

a first spacer insulating layer having a first deposition distribution that varies as a function of a location of said split gate flash memory cell on said substrate; and

a second spacer insulating layer, located over said first spacer insulating layer, having a second deposition distribution that varies in substantial opposition to said first deposition distribution of said first spacer insulating layer as a function of said location of said split gate flash memory cell on said substrate.

2. (Original) The composite spacer as recited in Claim 1 wherein said composite spacer forms a composite floating gate spacer proximate a floating gate of said split gate flash memory cell.

3. (Original) The composite spacer as recited in Claim 1 wherein said first spacer insulating layer forms a thicker composition proximate a center of said substrate and a thinner composition toward an edge of said substrate and said second spacer insulating layer forms a thinner composition proximate said center of said substrate and a thicker composition toward said edge of said substrate.

4. (Original) The composite spacer as recited in Claim 1 wherein said split gate flash memory cell is located proximate a center of said substrate, said first spacer insulating layer

having a thicker composition and said second spacer insulating layer having a thinner composition.

5. (Original) The composite spacer as recited in Claim 1 wherein said first spacer insulating layer is formed by a low pressure tetracthyl orthosilicate layer and said second spacer insulating layer is formed by a plasma enhanced tetraethyl orthosilicate layer.

6. (Currently Amended) A method of forming a composite spacer for use with a split gate flash memory cell on a substrate, comprising:

providing a first spacer insulating layer having a first deposition distribution that varies as a function of a location of said split gate flash memory cell on said substrate; and

~~depositing~~ providing a second spacer insulating layer over said first spacer insulating layer, ~~said second spacer insulating layer~~ and having a second deposition distribution that varies in substantial opposition to said first deposition distribution of said first spacer insulating layer as a function of said location of said split gate flash memory cell on said substrate.

7. (Original) The method as recited in Claim 6 wherein said composite spacer forms a composite floating gate spacer proximate a floating gate of said split gate flash memory cell.

8. (Original) The method as recited in Claim 6 wherein said first spacer insulating layer forms a thicker composition proximate a center of said substrate and a thinner composition toward an edge of said substrate and said second spacer insulating layer forms a thinner

composition proximate said center of said substrate and a thicker composition toward said edge of said substrate.

9. (Original) The method as recited in Claim 6 wherein said split gate flash memory cell is located proximate a center of said substrate, said first spacer insulating layer having a thicker composition and said second spacer insulating layer having a thinner composition.

10. (Original) The method as recited in Claim 6 wherein said first spacer insulating layer is formed by a low pressure tetraethyl orthosilicate layer and said second spacer insulating layer is formed by a plasma enhanced tetraethyl orthosilicate layer.

11. (Original) A split gate flash memory cell, comprising:

a substrate;

a substrate insulating layer located over said substrate;

a floating gate located over said substrate insulating layer;

a floating gate insulating layer located over said floating gate; and

a composite floating gate spacer, including:

a first spacer insulating layer, located over said floating gate insulating layer, having a first deposition distribution that varies as a function of a location of said split gate flash memory cell on said substrate, and

a second spacer insulating layer, located over said first spacer insulating layer, having a second deposition distribution that varies in substantial opposition to said first

deposition distribution of said first spacer insulating layer as a function of said location of said split gate flash memory cell on said substrate.

12. (Original) The split gate flash memory cell as recited in Claim 11, further comprising:

a coupling spacer that extends between said floating gate and said substrate insulating layer adjacent a source of said split gate flash memory cell; and

a composite contact spacer overlying said coupling spacer.

13. (Original) The split gate flash memory cell as recited in Claim 12, further comprising:

a common source line located adjacent said composite floating gate spacer and composite contact spacer and overlying said source;

a tunneling insulating layer located adjacent said composite floating gate spacer on an opposing side from said common source line;

a control gate located adjacent said tunneling insulating layer; and

a drain about said control gate and recessed into said substrate.

14. (Original) The split gate flash memory cell as recited in Claim 11 wherein said first spacer insulating layer forms a thicker composition proximate a center of said substrate and a thinner composition toward an edge of said substrate and said second spacer insulating layer forms a thinner composition proximate said center of said substrate and a thicker composition toward said edge of said substrate.

15. (Original) The split gate flash memory cell as recited in Claim 11 wherein said first spacer insulating layer is formed by a low pressure tetraethyl orthosilicate layer and said second spacer insulating layer is formed by a plasma enhanced tetraethyl orthosilicate layer.

16. (Original) A method of forming a split gate flash memory cell, comprising:

providing a substrate;

forming a substrate insulating layer over said substrate;

forming a floating gate over said substrate insulating layer;

forming a floating gate insulating layer over said floating gate; and

forming a composite floating gate spacer, including:

depositing a first spacer insulating layer over said floating gate insulating layer, said first spacer insulating layer having a first deposition distribution that varies as a function of a location of said split gate flash memory cell on said substrate, and

depositing a second spacer insulating layer over said first spacer insulating layer, said second spacer insulating layer having a second deposition distribution that varies in substantial opposition to said first deposition distribution of said first spacer insulating layer as a function of said location of said split gate flash memory cell on said substrate.

17. (Original) The method as recited in Claim 16, further comprising:

forming a coupling spacer between said floating gate and a source of said split gate flash memory cell; and

forming a composite contact spacer over said coupling spacer.

18. (Original) The method as recited in Claim 17, further comprising:

forming a common source line adjacent said composite floating gate spacer and composite contact spacer and overlying said source;

forming a tunneling insulating layer adjacent said composite floating gate spacer on an opposing side from said common source line;

forming a control gate adjacent said tunneling insulating layer; and

forming a drain about said control gate and recessed into said substrate.

19. (Original) The method as recited in Claim 16 wherein said first spacer insulating layer forms a thicker composition proximate a center of said substrate and a thinner composition toward an edge of said substrate and said second spacer insulating layer forms a thinner composition proximate said center of said substrate and a thicker composition toward said edge of said substrate.

20. (Original) The method as recited in Claim 16 wherein said first spacer insulating layer is formed by a low pressure tetraethyl orthosilicate layer and said second spacer insulating layer is formed by a plasma enhanced tetraethyl orthosilicate layer.

21. (Original) A composite spacer for use with a split gate flash memory cell on a substrate, comprising:

a first spacer insulating layer having a substantially uniform deposition distribution across a surface thereof; and

a second spacer insulating layer, located over said first spacer insulating layer, having a varying deposition distribution across a surface thereof, said second spacer insulating layer having a thinner composition in selected regions of said split gate flash memory cell thereby reducing an over etch time associated with an etching process to form said composite spacer.

22. (Original) The composite spacer as recited in Claim 21 wherein said composite spacer forms a composite contact spacer proximate a composite floating gate spacer of said split gate flash memory cell.

23. (Original) The composite spacer as recited in Claim 21 wherein said selected region is a narrow region between composite floating gate spacers of said split gate flash memory cell, said second spacer insulating layer having a thinner composition therebetween.

24. (Original) The composite spacer as recited in Claim 21 wherein said first spacer insulating layer is formed by a hot temperature oxide layer.

25. (Original) The composite spacer as recited in Claim 21 wherein said second spacer insulating layer is formed by a resist protect oxide layer.

26. (Currently Amended) A method of forming a composite spacer for use with a split gate flash memory cell on a substrate, comprising:

providing a first spacer insulating layer having a substantially uniform deposition distribution across a surface thereof; and

~~depositing~~ providing a second spacer insulating layer over said first spacer insulating layer, said second spacer insulating layer having a varying deposition distribution across a surface thereof, said second spacer insulating layer having a thinner composition in selected regions of said split gate flash memory cell thereby reducing an over etch time associated with an etching process to form said composite spacer.

27. (Original) The method as recited in Claim 26 wherein said composite spacer forms a composite contact spacer proximate a composite floating gate spacer of said split gate flash memory cell.

28. (Original) The method as recited in Claim 26 wherein said selected region is a narrow region between composite floating gate spacers of said split gate flash memory cell, said second spacer insulating layer having a thinner composition therebetween.

29. (Original) The method as recited in Claim 26 wherein said first spacer insulating layer is formed by a hot temperature oxide layer.

30. (Original) The method as recited in Claim 26 wherein said second spacer insulating layer is formed by a resist protect oxide layer.

31. (Original) A split gate flash memory cell, comprising:

a substrate;

a substrate insulating layer located over said substrate;

a floating gate located over said substrate insulating layer;

a floating gate insulating layer located over said floating gate; and

a composite contact spacer located proximate said floating gate, including:

a first spacer insulating layer having a substantially uniform deposition distribution across a surface thereof, and

a second spacer insulating layer, located over said first spacer insulating layer, having a varying deposition distribution across a surface thereof, said second spacer insulating layer having a thinner composition in selected regions of said split gate flash memory cell thereby reducing an over etch time associated with an etching process to form said composite contact spacer.

32. (Original) The split gate flash memory cell as recited in Claim 31, further comprising:

a coupling spacer that extends between said floating gate and said substrate insulating layer adjacent a source of said split gate flash memory cell and underlying said composite contact spacer; and

a composite floating gate spacer located over said floating gate insulating layer.

33. (Original) The split gate flash memory cell as recited in Claim 32, further comprising:

a common source line located adjacent said composite floating gate spacer and composite contact spacer and overlying said source;

a tunneling insulating layer located adjacent said composite floating gate spacer on an opposing side from said common source line;

a control gate located adjacent said tunneling insulating layer; and

a drain about said control gate and recessed into said substrate.

34. (Original) The split gate flash memory cell as recited in Claim 31 wherein said selected region is a narrow region adjacent a composite floating gate spacer of said split gate flash memory cell, said second spacer insulating layer having a thinner composition therebetween.

35. (Original) The split gate flash memory cell as recited in Claim 31 wherein said first spacer insulating layer is formed by a hot temperature oxide layer and said second spacer insulating layer is formed by a resist protect oxide layer.

36. (Original) A method of forming a split gate flash memory cell, comprising:

providing a substrate;

forming a substrate insulating layer over said substrate;

forming a floating gate over said substrate insulating layer;

forming a floating gate insulating layer over said floating gate; and

forming a composite contact spacer proximate said floating gate, including:

providing a first spacer insulating layer having a substantially uniform deposition distribution across a surface thereof, and

depositing a second spacer insulating layer over said first spacer insulating layer, said second spacer insulating layer having a varying deposition distribution across a

surface thereof, said second spacer insulating layer having a thinner composition in selected regions of said split gate flash memory cell thereby reducing an over etch time associated with an etching process to form said composite contact spacer.

37. (Original) The method as recited in Claim 36, further comprising:

forming a coupling spacer between said floating gate and a source of said split gate flash memory cell and underlying said composite contact spacer; and

forming a composite floating gate spacer over said floating gate insulating layer.

38. (Original) The method as recited in Claim 37, further comprising:

forming a common source line adjacent said composite floating gate spacer and composite contact spacer and overlying said source;

forming a tunneling insulating layer adjacent said composite floating gate spacer on an opposing side from said common source line;

forming a control gate adjacent said tunneling insulating layer; and

forming a drain about said control gate and recessed into said substrate.

39. (Original) The method as recited in Claim 36 wherein said selected region is a narrow region adjacent a composite floating gate spacer of said split gate flash memory cell, said second spacer insulating layer having a thinner composition therebetween.

40. (Original) The method as recited in Claim 36 wherein said first spacer insulating layer is formed by a hot temperature oxide layer and said second spacer insulating layer is formed by a resist protect oxide layer.

41. (Original) A coupling spacer for use with a split gate flash memory cell on a substrate having a substrate insulating layer thereon comprising a conductive layer that extends between a floating gate and said substrate insulating layer adjacent a source recessed into said substrate of said split gate flash memory cell thereby increasing a coupling area between said floating gate and said source.

42. (Original) The coupling spacer as recited in Claim 41 wherein said conductive layer is doped polycrystalline silicon.

43. (Original) The coupling spacer as recited in Claim 42 wherein said doped polycrystalline silicon has a thickness of about 200 angstroms.

44. (Original) The coupling spacer as recited in Claim 41 wherein said coupling spacer is located proximate a composite floating gate spacer of said split gate flash memory cell.

45. (Original) The coupling spacer as recited in Claim 41 wherein said coupling spacer underlies a composite contact spacer of said split gate flash memory cell.

46. (Original) A method of forming a coupling spacer for use with a split gate flash memory cell on a substrate having a substrate insulating layer thereon comprising forming a conductive layer that extends between a floating gate and said substrate insulating layer adjacent a source recessed into said substrate of said split gate flash memory cell thereby increasing a coupling area between said floating gate and said source.

47. (Original) The method as recited in Claim 46 wherein said conductive layer is doped polycrystalline silicon.

48. (Original) The method as recited in Claim 47 wherein said doped polycrystalline silicon has a thickness of about 200 angstroms.

49. (Original) The method as recited in Claim 46 wherein said coupling spacer is located proximate a composite floating gate spacer of said split gate flash memory cell.

50. (Original) The method as recited in Claim 46 wherein said coupling spacer underlies a composite contact spacer of said split gate flash memory cell.

51. (Original) A split gate flash memory cell, comprising:

a substrate;

a source recessed into said substrate;

a substrate insulating layer located over said substrate;

a floating gate located over said substrate insulating layer;

a floating gate insulating layer located over said floating gate; and

a coupling spacer including a conductive layer that extends between said floating gate and said substrate insulating layer adjacent said source thereby increasing a coupling area between said floating gate and said source.

52. (Original) The split gate flash memory cell as recited in Claim 51, further comprising:

a composite floating gate spacer located over said floating gate insulating layer; and

a composite contact spacer located proximate said composite floating gate spacer.

53. (Original) The split gate flash memory cell as recited in Claim 52, further comprising:

a common source line located adjacent said composite floating gate spacer and composite contact spacer and overlying said source;

a tunneling insulating layer located adjacent said composite floating gate spacer on an opposing side from said common source line;

a control gate located adjacent said tunneling insulating layer; and

a drain about said control gate and recessed into said substrate.

54. (Original) The split gate flash memory cell as recited in Claim 51 wherein said conductive layer is doped polycrystalline silicon having a thickness of about 200 angstroms.

55. (Original) The split gate flash memory cell as recited in Claim 51 wherein said coupling spacer underlies a composite contact spacer of said split gate flash memory cell.

56. (Original) A method of forming a split gate flash memory cell, comprising:

providing a substrate;

forming a source recessed into said substrate;

forming a substrate insulating layer over said substrate;

forming a floating gate over said substrate insulating layer;

forming a floating gate insulating layer over said floating gate; and

forming a coupling spacer including a conductive layer that extends between said floating gate and said substrate insulating layer adjacent said source thereby increasing a coupling area between said floating gate and said source.

57. (Original) The method as recited in Claim 56, further comprising:

forming a composite floating gate spacer over said floating gate insulating layer; and

forming a composite contact spacer proximate said composite floating gate spacer.

58. (Original) The method as recited in Claim 57, further comprising:

forming a common source line adjacent said composite floating gate spacer and composite contact spacer and overlying said source;

forming a tunneling insulating layer adjacent said composite floating gate spacer on an opposing side from said common source line;

forming a control gate adjacent said tunneling insulating layer; and

forming a drain about said control gate and recessed into said substrate.

59. (Original) The method as recited in Claim 56 wherein said conductive layer is doped polycrystalline silicon having a thickness of about 200 angstroms.

60. (Original) The method as recited in Claim 56 wherein said coupling spacer underlies a composite contact spacer of said split gate flash memory cell.